APJ Abdul Kalam Technological University

Cluster 4: Kottayam

M. Tech Program in Electronics & Communication Engineering
(Advanced Electronics & Communication)

Scheme of Instruction & Syllabus: 2015 Admissions

Compiled By
Rajiv Gandhi Institute of Technology, Kottayam
July 2015
APJ Abdul Kalam Technological University  
(Kottayam Cluster)  
M. Tech in Electronics and Communication Engineering  
With specialization in Advanced Electronics and Communication Engineering

Scheme

Credit requirements: 65 credits (21+18+14+12)  
Normal Duration: Regular: 4 semesters; External Registration: 6 semesters;  
Maximum duration: Regular: 6 semesters; External Registration: 7 semesters.

Courses: Core Courses: Either 4 or 3 credit courses; Elective courses: All of 3 credits

ELIGIBILITY: B. Tech / B.E in Electronics and Communication engineering, or allied branches with strong focus in electronics engineering.

Allotment of credits and examination scheme:-

Semester 1

<table>
<thead>
<tr>
<th>Exam Slot</th>
<th>Course No:</th>
<th>Name</th>
<th>L-T-P</th>
<th>Internal Marks</th>
<th>End Semester Exam</th>
<th>Credits</th>
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<td>A</td>
<td>04 EC 6101</td>
<td>Linear Algebra for Communication Engg</td>
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<td>B</td>
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<td>Probability and Random Processes</td>
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<td>C</td>
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<td>Design of CMOS VLSI Circuits</td>
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<td>D</td>
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<td>40</td>
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<td>E</td>
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*See List of Electives-I for slot E

List of Elective - I Courses

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<tr>
<td>E</td>
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<td>Detection and Estimation Techniques</td>
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<tr>
<td>E</td>
<td>04 EC 6207</td>
<td>Synthesis of Digital Systems</td>
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<td>E</td>
<td>04 EC 6209</td>
<td>FPGA Based System Design</td>
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<tr>
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<td>Image &amp; Video Processing</td>
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**Semester 2 (Credits: 18)**

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<td>40</td>
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<td>C</td>
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*See List of Electives -II for slot D

**List of Elective - II Courses**

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**List of Elective - III Courses**

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*See List of Electives -III for slot E*
Semester 3 (Credits: 14)

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List of Elective - IV Courses

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<td>VLSI Structures for DSP</td>
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<td>04 EC 7205</td>
<td>Advanced Digital System Design Techniques</td>
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<td>A</td>
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<td>Pattern Recognition</td>
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List of Elective - V Courses

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<tr>
<td>B</td>
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<td>VLSI Subsystem Design</td>
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<tr>
<td>B</td>
<td>04 EC 7211</td>
<td>Testing of VLSI Circuits</td>
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<td>B</td>
<td>04 EC 7213</td>
<td>Advanced Digital Communication</td>
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<td>Recent Trends in Communication Engineering</td>
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Semester 4 (Credits: 12)

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Total: 65
Pre-requisites: Nil

Course Objectives:

- To gain an understanding of the linear system of equations
- To get introduced to the fundamentals of vector spaces
- To impart the basics of linear transformation, inner product spaces and orthogonalization
- To provide the knowledge to apply linear algebra in communication engineering

Syllabus

Introduction to linear system, matrices, vector spaces, Triangular factors and row exchanges (LU), Linear Transformation, Orthogonality, Hilbert spaces, orthogonal complements, projection theorem, orthogonal projections, Eigen values, eigen vectors, diagonalization, symmetric matrices, Least-square solution of inconsistent system, singular value decomposition, selected topics in communication Engg.

Course Outcome:

Students who successfully complete this course would have the ability to solve the problems related to linear systems and matrices- Apply the knowledge of linear transformation, orthogonal projections and orthonormalization to engineering applications-to obtain the Least-square solution of inconsistent system -to apply singular value decomposition in typical applications.

Text Books:

1. K. Hoffman, R. Kunz, “Linear Algebra”, Prentice Hall India

References:

2. Gareth Williams, “Linear algebra with applications”, Narosa
## COURSE PLAN

<table>
<thead>
<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<td>04 EC 6101</td>
<td>LINEAR ALGEBRA FOR COMMUNICATION ENGG</td>
<td>4-0-0:4</td>
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### MODULES

<table>
<thead>
<tr>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
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**MODULE 1:** Matrices: Introduction to linear system, matrices, vectors. Gaussian elimination, matrix notation, partitioned matrices, multiplication of partitioned matrices, inverse of partitioned matrices

- **Contact Hours:** 8
- **Sem. Exam Marks (%):** 15

**MODULE 2:** Triangular factors and row exchanges (LU) Row exchanges and permutation matrices, inverses (Gauss-Jordan method)

- **Contact Hours:** 6
- **Sem. Exam Marks (%):** 15

**INTERNAL TEST 1 (MODULE 1 & 2)**

- **Contact Hours:** 10
- **Sem. Exam Marks (%):** 15

**MODULE 3:** Vector space, subspace, linear independence, span, basis, dimension. Spanning set theorem, null space, column space, row space-(Matrix) Basis and dimension of null space, column space, row space-(Matrix) Rank nullity theorem, co-ordinate system, change of basis–(finite space)

- **Contact Hours:** 10
- **Sem. Exam Marks (%):** 15

**INTERNAL TEST 2 (MODULE 3 & 4)**

- **Contact Hours:** 10
- **Sem. Exam Marks (%):** 15

**MODULE 4:** Linear transformation, Kernel and range of linear transformation, matrix representation of linear transform, inverse transform, Inner product spaces: Inner product space, norm, Cauchy-Schwarz inequality, Triangular inequality, self adjoint and normal operators

- **Contact Hours:** 8
- **Sem. Exam Marks (%):** 20

**MODULE 5:** Orthogonality, Hilbert spaces, orthogonal complements, projection theorem, orthogonal projections

- **Contact Hours:** 8
- **Sem. Exam Marks (%):** 20

**MODULE 6:** Eigen values, eigen vectors, diagonalization, symmetric matrices Quadratic forms, classification of quadratic forms. Least-square solution of inconsistent system, singular value decomposition. Application of SVD in OFDM communication system. Application of Gram-Schmidt orthogonalization in signal space representation of digital modulation schemes

- **Contact Hours:** 14
- **Sem. Exam Marks (%):** 20

**END SEMESTER EXAM**
Pre-requisites: Nil

Course Objectives

- To introduce the fundamentals of probability theory and random processes
- To study limit theorems and stochastic processes
- To learn the important concepts of random processes and to apply it to communication systems

Syllabus

Introduction to Probability Theory - conditional probabilities, - Bayes’ theorem.

Course Outcome:

Students finishing this course will have the ability

- to model communication systems based on random process
- to understand limit theorems and stochastic processes
- to deal with probability and random processes

Text books

1. V. Sundarapandian, “Probability, statistics and Queueing theory”, Prentice Hall of India

References:


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### MODULES

| MODULE 1: Introduction to Probability Theory | Samplespace and events, conditional probabilities, independent events, the law of total probability and Bayes’ theorem, Random variables: Discrete and continuous random variables, distributions, expectation of a random variable | 8 | 15 |
| MODULE 2: Moment generating function, joint probability distributions, marginal probability distributions and random vectors, Markov and Chebyshev inequalities, Weak and strong law of large numbers, convergence concepts and central limit theorem | 6 | 15 |

**INTERNAL TEST 1 (MODULE 1 & 2)**

| MODULE 3: Stochastic process (definition), conditional probability distributions (continuous and discrete cases), computing mean and variances by conditioning. | 7 | 15 |
| MODULE 4: Random process - Classification of random process, special classes of random process, SSS and WSS, auto and cross-correlation, Ergodicity, Mean ergodic process, power spectral density | 7 | 15 |

**INTERNAL TEST 2 (MODULE 3 & 4)**

| MODULE 5: Unit impulse response system, response of a LTI system to WSS input, noise in communication system-white Gaussian noise, filters. | 7 | 20 |

**END SEMESTER EXAM**
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
---|---|---|---
04 EC 6201 | DESIGN OF CMOS VLSI CIRCUITS | 3-0-0: 3 | 2015

Pre-requisites: Nil

Objectives

- To introduce the basics of logic design in CMOS technology.
- To introduce to the physical design of Integrated Circuits.
- To introduce to VLSI Testing.

Syllabus

- MOSFETs-characteristics - MOS Capacitances - MOS RC Model
- Analysis of CMOS logic gates
- BiCMOS Circuits - Scaling of MOS circuits
- VLSI Circuit Design Processes - CMOS Design rules
- Gate Level Design - driving large capacitive load
- logical effort - optimizing the number of stages
- BiCMOS drivers
- Wiring capacitance, interconnect delays
- Static & Dynamic CMOS design
- CMOS Testing

Course Outcome:

Students finishing this course will have the ability

- to understand MOSFET characteristics and MOS Capacitances
- to analyse CMOS logic gates
- to design for large capacitive loads

Text books


References:

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<th>COURSE TITLE</th>
<th>CREDITS</th>
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<td>04 EC 6201</td>
<td>Design Of CMOS VLSI Circuits</td>
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**MODULES**

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<tr>
<th>Contact Hours</th>
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**MODULE 1:** Electrical characteristics of MOSFETs: MOS physics, threshold voltage, current-voltage equations, Body bias effects, Nonideal I-V effects, Nonideal I-V effects. MOS Capacitances, MOS RC Model.

- **MODULE 2:** Analysis of CMOS logic gates: Switching characteristics, DC characteristics, Power dissipation of CMOS Inverter, NAND & NOR gates, Analysis of complex logic gates – gate design for transient response Analysis and Design of BiCMOS Circuits. Scaling of MOS circuits, limitations of scaling.

**INTERNAL TEST 1 (MODULE 1 & 2)**

- **MODULE 3:** VLSI design flow, Elements of Physical design -MOS layers, stick diagrams, design rules and layout, Layout for basic structures, CMOS Design rules for wires, Contacts and transistors, layout diagrams for NMOS and CMOS inverters and gates.

- **MODULE 4:** Basic circuit concepts, sheet resistance and its concept to MOS, area capacitance.Gate delays - driving large capacitive load, Delay minimization in an inverter cascade.

**INTERNAL TEST 2 (MODULE 3 & 4)**

- **MODULE 5:** Logical effort – basic definitions, optimizing the number of stages BiCMOS drivers. Wiring capacitance, interconnect delays. Static & Dynamic CMOS design.

- **MODULE 6:** CMOS testing - Need for testing, test principles, design strategies for test. Chip level test techniques, system level test techniques, layout design for improved testability Application of SVD in OFDM communication system. Application of Gram-Schmidt orthogonalization in signal space representation of digital modulation schemes.

**END SEMESTER EXAM**
Pre-requisites: Nil

Course Objectives:

To give the Student:

- To provide students with a sound understanding of existing Digital Signal Processors
- To develop an understanding of the need for parallelism.
- To introduce different number systems in computer arithmetic
- To develop the basic tools with which students can later learn about newly developed processors and its various applications.

Syllabus

Introduction to DSP processors, Pipeline and introduction to memory, Instruction Level Parallelism (ILP), Computer arithmetic, Case studies, Implementation using MATLAB

Course Outcome:

Students who successfully complete this course will have demonstrated an ability to understand the fundamental concepts DSP Processors; Apply the basic concepts of pipelining, parallelism and computer arithmetic and implementation using MATLAB

Text books


References:

4. User’s manual for of various fixed and floating point DSPs, TMS320C6x Data Sheets from TI. Blackfin Processor Hardware Reference, Analog Devices, Version 3.0, 2004
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<td>DSP Algorithms And Architectures</td>
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<th>MODULES</th>
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<tr>
<td><strong>MODULE 1:</strong> Need for special DSP processors, von Neumann versus Harvard Architecture, Architectures of superscalar and VLIW fixed and floating point processors, Review of pipelined RISC, architecture and instruction set design, performance and benchmarks-SPEC CPU 2000</td>
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| **MODULE 2:** EEMBC DSP benchmarks, basic pipeline: implementation details, pipeline hazards (based on MIPS 4000 arch), review of memory hierarchy – cache design, cache performance issues & improving techniques |
| Contact Hours | Sem. Exam Marks (%) |
| 7 | 15 |

**INTERNAL TEST 1 (MODULE 1 & 2)**

| **MODULE 3:** Concepts, dynamic scheduling - reducing data hazards, dynamic hardware prediction - reducing branch hazards, multiple issue- hardware-based speculation, limitations of ILP |
| Contact Hours | Sem. Exam Marks (%) |
| 7 | 15 |

| **MODULE 4:** Computer arithmetic: Signed digit numbers (SD), multiplier adder graph, Logarithmic and Residue Number system (LNS, RNS), index multiplier, pipelined adders, modulo adders, Distributed Arithmetic (DA) - CORDIC Algorithm |
| Contact Hours | Sem. Exam Marks (%) |
| 9 | 15 |

**INTERNAL TEST 2 (MODULE 3 & 4)**

| **MODULE 5:** Case studies: Introduction to architecture Details of (a) BlackFin processor (Analog Devices) (b) TMS320C64X Digital Signal Processing Applications: FIR and IIR Digital Filter Design, Filter Design Programs using MATLAB |
| Contact Hours | Sem. Exam Marks (%) |
| 6 | 20 |

| **MODULE 6:** Fourier Transform: DFT, FFT programs using MATLAB - Real Time Implementation on DSP processors- Factors to be considered for optimized implementation based on processor architecture: Implementation of simple Real Time Digital Filters, FFT using DSP [Only familiarity with instruction set is expected. It is not required to memorize all the instructions.]. |
| Contact Hours | Sem. Exam Marks (%) |
| 6 | 20 |

**END SEMESTER EXAM**
### ELECTIVE-1

<table>
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<td>DETECTION AND ESTIMATION TECHNIQUES</td>
<td>3-0-0: 3</td>
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**Pre-requisites:** Nil

**Course Objectives:**

- To impart the fundamentals of estimation and detection theory;
- To learn various types of estimators and their performance bounds;
- To introduce the various decision rules in detection theory;

**Syllabus**

Estimation theory and it’s mathematical formulation; Linear models and least Squares; Extension to vector parameter and application examples; Detection theory and it’s mathematical formulation; Detection of deterministic and random signals in noise; Bayesian approach in detection.

**Course Outcome:**

Students who successfully complete this course will understand the fundamentals of estimation and detection theory. This helps the students to mathematically model the communication systems. Also, the knowledge of various types of estimators and decision rules obtained from the course enables them to design and implement better communication receivers.

**Text Books:**


**References:**

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<tbody>
<tr>
<td>MODULE : 1 Estimation Theory-Mathematical formulation of Parameter Estimation, Minimum Variance Unbiased Estimation (MVUE), Cramer-Rao Lower Bound (CRLB), CRLB for signals in White Gaussian Noise, extension to vector parameter, application examples.</td>
<td>7</td>
<td>15</td>
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<tr>
<td>MODULE : 2 Best Linear Unbiased Estimation (BLUE), Maximum likelihood estimation (MLE), extension to vector parameter, application examples.</td>
<td>7</td>
<td>15</td>
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<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
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</tr>
<tr>
<td>MODULE : 3 Least Squares, Method of Moments, Bayesian estimators, extension to vector parameter, application examples.</td>
<td>7</td>
<td>15</td>
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<tr>
<td>MODULE : 4 Detection Theory-Mathematical formulation, Hypothesis Testing, Neyman Pearson Theorem, Bayes criterion, minimum probability of error criterion, likelihood ratio test, application examples.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td></td>
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<tr>
<td>MODULE : 5 Detection of deterministic and random signals in noise, Composite Hypothesis Testing, generalized likelihood ratio test, application examples.</td>
<td>7</td>
<td>20</td>
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<tr>
<td>MODULE : 6 Bayesian approach in detection, detection of deterministic and random signals with unknown parameters, application examples.</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>END SEMESTER EXAM</td>
<td></td>
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</tr>
</tbody>
</table>
Pre-requisites: Nil

Course Objectives:

To give the Student:-

- To impart a thorough knowledge about the need for logic level minimizations
- To provide basic knowledge about FSM network and its minimization
- To study and design algorithmic state machines

Syllabus

Two Level Minimization, Multi Level Minimization, Multi-Level Logic Synthesis, Sequential Logic Synthesis, Synthesis at the Register Transfer Level, Implementation of digital systems.

Course Outcome:

Students who successfully complete this course will have demonstrated an ability to understand the fundamental concepts minimizing Boolean expressions using two level and multi level techniques; To provide an insight into synthesis process and implementation

Text books


References:

### COURSE CODE: 04 EC 6207  
### COURSE TITLE: Synthesis Of Digital Systems  
### CREDITS: 3-0-0:3

<table>
<thead>
<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 1: Two Level Minimization  Introduction- logic functions and their representation, Unate functions/recursive paradigm, Quine-McCluskey, ESPRESSO two level minimization</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Multivalued Minimization BDDs- Introduction (Boolean networks, factored forms) division, simplification, full simplify SPFDs</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td></td>
<td></td>
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<tr>
<td>MODULE 3: Multi-Level Logic Synthesis- Technology mapping, timing optimization application to special logic implementation styles.</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Sequential Logic Synthesis- Introduction (FSM networks), node minimization, state minimization, retiming and resynthesis verification, state assignment.</td>
<td>8</td>
<td>15</td>
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<tr>
<td>END SEMESTER EXAM</td>
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<td></td>
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</tbody>
</table>

**NOTE:** The table entries under Contact Hours and Sem. Exam Marks (%) are subject to change based on specific course requirements and updates.
Pre-requisites: Nil

Course Objectives:

To give the Student:-

- To learn the various programmable devices and their architecture
- To learn its technology mapping and routing

Syllabus

Evolution of Programmable Devices, FPGA Technology, FPGA and Design Process, Technology Mapping for FPGAs, Mapping for FPGAs, Routing of FPGAs

Course Outcome:

Apply the basics of programmable devices, FPGA technology and design process. Students who successfully complete this course will get an idea of mapping and routing FPGAs;

Text books


References

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<th>COURSE CODE:</th>
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</thead>
<tbody>
<tr>
<td>04 EC 6209</td>
<td>FPGA Based System Design</td>
<td>3-0-0:3</td>
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<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 1: Evolution of Programmable Devices - Introduction to AND-OR structured Programmable Logic Devices, PROM, PLA, PAL and MPGAs, Combinational and sequential circuit realization using PROM based Programmable Logic Element (PLE), architecture of FPAD, F PLA, FPLS and FPID devices.</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: FPGA Technology - FPGA resources - Logic Blocks and Interconnection Resources, Economics and applications of FPGAs, Implementation Process for FPGAs Programming Technologies, Static RAM Programming, Anti Fuse Programming, EPROM and EEPROM Programming Technology</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODULE 3: FPGA and Design Process - commercially available FPGAs - Xilinx FPGAs, Altera FPGAs, FPGA. Design Flow Example - Initial Design Entry, Translation to XNF Format, Partitioning, Place and Route, Performance Calculation and Design Verification.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Technology Mapping for FPGAs - Logic Synthesis - Logic Optimization and Technology Mapping, Lookup Table Technology Mapping - Chortle-crf Technology Mapper, Chortle-d Technology Mapper, Lookup Table Technology Mapping in mis-pga</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODULE 5: Mapping for FPGAs - Lookup Table Technology Mapping in Asyl and Hydra Technology Mapper; Multiplexer Technology Mapping - Multiplexer Technology Mapping in mis-pga. Design Flow Example - Initial Design Entry, Translation to XNF Format, Partitioning, Place and Route, Performance Calculation and Design Verification.</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>MODULE 6: Routing for FPGAs - Routing Terminology; Strategy for routing in FPGAs; Routing for Row- Based FPGAs. Logic Block Architecture: Logic Block Functionality versus Area-Efficiency - Logic Block Selection, Experimental Procedure, Logic Block Area and Routing Model and Results. - Segmented channel routing, 1-channel routing algorithm, K – channel routing algorithm and results.</td>
<td>7</td>
<td>20</td>
</tr>
</tbody>
</table>

END SEMESTER EXAM
Pre-requisites: Nil

Objectives:

- To introduce the fundamental concepts of digital image processing and applications
- To familiarize the various techniques in image enhancement
- To impart the fundamentals in boundary description and video processing

Syllabus


Course Outcome:

Students finishing this course will have the ability

- to understand the fundamental concepts of digital image processing and applications
- to analyse and perform image enhancement and segmentation problems
- to perform Image Compression techniques

Text books


References

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<td>04 EC 6113</td>
<td>Image And Video Processing</td>
<td>3-0-0:3</td>
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<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 1: Introduction to Digital Image Processing &amp; Applications - Elements of visual perception, Mach band effect, sampling, quantization, basic relationship between pixels, color image fundamentals-RGB-HSI models</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Image transforms - two dimensional orthogonal and unitary transforms, separable unitary transforms, basis images, DFT, WHT, KLT, DCT and SVD</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
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</tr>
<tr>
<td>MODULE 3: Image Enhancement - Point operations, Spatial operations and Transform operations, histogram-based processing. Image restoration: degradation models, PSF, restoration using inverse filtering</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Wiener filtering, Image segmentation: bi-level thresholding, multilevel thresholding, adaptive thresholding, region growing, splitting and merging, edge detection and linking, Hough transform.</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODULE 5: Boundary Representation - Chain codes, polygonal approximation, boundary segments, boundary descriptors, regional descriptors, relational descriptors, Object recognition, pattern and pattern classes Recognition based on decision theoretic methods, matching, optimum statistical classifiers. Morphological image processing, erosion and dilation, opening or closing, HIT or MISS transformation, basic morphological algorithms.</td>
<td>8</td>
<td>20</td>
</tr>
</tbody>
</table>

END SEMESTER EXAM
Pre-requisites: Nil

Objectives:

- To get introduced to research philosophy and processes in general.
- To formulate the research problem and prepare research plan.
- To apply various numerical/quantitative techniques for data analysis
- To communicate the research findings effectively

Syllabus

Introduction to the Concepts of Research Methodology, Research Proposals, Research Design, Data Collection and Analysis, Quantitative Techniques and Mathematical Modeling, Report Writing

Course Outcome:

Students who successfully complete this course would learn the fundamental concepts of Research Methodology, apply the basic aspects of the Research methodology to formulate a research problem and its plan. They would also be able to deploy numerical/quantitative techniques for data analysis. They would be equipped with good technical writing and presentation skills.

Text books

1. Research Methodology: ‘Methods and Techniques’, by Dr. C. R. Kothari, New Age International Publisher, 2004
2. Research Methodology: A Step by Step Guide for Beginners’ by Ranjit Kumar, SAGE Publications Ltd; Third Edition

Reference Books:

2. Research Methodology: An Introduction’ by Wayne Goddard and Stuart Melville, Juta and Company Ltd, 2004
<table>
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<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<tbody>
<tr>
<td>04 GN 6001</td>
<td>Research Methodology</td>
<td>0-2-0:2</td>
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| MODULES | Contact Hours | Sem. Exam Marks (%)
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<tr>
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<tbody>
<tr>
<td>MODULE 1: Introduction to Research Methodology, Concepts of Research, Meaning and Objectives of Research, Research Process, Types of Research, Type of research: Descriptive vs. Analytical, Applied vs. Fundamental, Quantitative vs. Qualitative, and Conceptual vs. Empirical</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Criteria of Good Research, Research Problem, Selection of a problem, Techniques involved in definition of a problem, Research Proposals – Types, contents, Ethical aspects, IPR issues like patenting, copyrights.</td>
<td>4</td>
<td>15</td>
</tr>
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</table>

**INTERNAL TEST 1 (MODULE 1 & 2)**

| MODULE 3: Meaning, Need and Types of research design, Literature Survey and Review, Identifying gap areas from literature review, Research Design Process, Sampling fundamentals, Measurement and scaling techniques, Data Collection – concept, types and methods, Design of Experiments. | 5 | 15 |
| MODULE 4: Probability distributions, Fundamentals of Statistical analysis, Data Analysis with Statistical Packages, Multivariate methods, Concepts of correlation and regression, Fundamentals of time series analysis and spectral analysis | 5 | 15 |

**INTERNAL TEST 2 (MODULE 3 & 4)**

| MODULE 5: Principles of Thesis Writing, Guidelines for writing reports & papers, Methods of giving references and appendices, Reproduction of published material, Plagiarism, Citation and acknowledgement, | 5 | 20 |
| MODULE 6 : Documentation and presentation tools – LATEX, Office Software with basic presentations skills, Use of Internet and advanced search techniques | 4 | 20 |

**END SEMESTER EXAM**
Objective:

Each student shall present a seminar on any topic of interest related to the core/elective courses offered in the 1st semester of the M Tech Programme. He / She shall select the topic based on the references from international journals of repute, preferably IEEE journals. They should get the paper approved by the Programme Co-ordinator / Faculty member in charge of the seminar and shall present it in the class. Every student shall participate in the seminar. The students should undertake a detailed study on the topic and submit a report at the end of the semester. Marks will be awarded based on the topic, presentation, participation in the seminar and the report submitted.
COURSE CODE | COURSE NAME | L-T-P-C | YEAR
---|---|---|---
04 EC 6293 | DSP SYSTEMS LAB | 0-0-2: 1 | 2015

Pre-requisites: Nil

AIM:

To introduce the basic concepts of TMS 320C67XX DSP Kit and to give an exposure to Digital coding schemes.

OBJECTIVE:

- To familiarize the basic communication experiments using CCS and DSP Kit.
- Experiments for familiarizing basic probability functions.
- To analyse the Parameter estimators.
- To familiarize Different Digital Coding Schemes.

(Experiments are to be conducted using DSP kit)

1. Solution of Difference Equations
2. Impulse Response of IIR Filter
3. Linear Convolution
4. Circular Convolution
5. FIR Filter using Windowing
6. Pseudo-Random Binary Sequence Generation(Scrambling and Descrambling)
7. Effect of Aliasing
8. IIR Filter
9. Fast Fourier Transform
10. Noise Cancellation using Adaptive Filters
11. Spectrogram
12. Power Density Spectrum

Text books


Reference:

SEMESTER II

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>COURSE NAME</th>
<th>L-T-P:C</th>
<th>YEAR</th>
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</thead>
<tbody>
<tr>
<td>04 EC 6202</td>
<td>MULTIRATE SIGNAL PROCESSING AND WAVELETS</td>
<td>3 -0-0: 3</td>
<td>2015</td>
</tr>
</tbody>
</table>

Pre-requisites: Digital Signal Processing

Course Objectives:

- To impart the fundamental concepts of multirate Digital Signal Processing
- To introduce the various types of filter banks
- To explore the applications of multirate systems in communication
- To impart the basic concepts in STFT, wavelets and its application in communication

Syllabus

Fundamentals of Multirate Digital Signal Processing, Basic sampling rate alteration devices, Multirate identities, Filter banks, QMF filter banks Cosine modulated filter banks, Tree structured filter banks, Applications of multi-rate systems in communication, Short time Fourier Transform and Wavelets, Discrete Wavelet transform, Multi-resolution formulation of Wavelet systems and Wavelet applications, Filter banks and the DWT, Wavelet packets, Application of wavelet theory in communication systems.

Course Outcome:

Students who successfully completed this course would have gained an insight into the sampling rate alteration devices and the various types of filter banks. They would be also be able to apply the multi-rate theory in to typical engineering problems. They would be equipped with the knowledge of wavelet transform and its implementation using filter-banks, which would enable them to apply it in typical applications in communication engineering

Text books:

1. P P. Vaidyanathan, “Multirate Systems and Filter Banks”, Pearson Education

References:

2. Frederic J Harris. “Multirate Signal Processing for communication systems”, Pearson Education
<table>
<thead>
<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
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<tbody>
<tr>
<td>04 EC 6202</td>
<td>Multirate Signal Processing And Wavelets</td>
<td>3-0-0:3</td>
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<table>
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<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 1: Fundamentals of Multirate Digital Signal Processing - Basic sampling rate alteration devices-Sampling rate reduction by an integer factor: Down sampler - Time and frequency domain characterization of downsampler – Anti-aliasing filter and decimation system – Sampling rate increase by an integer factor. Upsampler – Time and frequency domain characterization of upsampler – Anti-imaging filter and interpolation system – Gain of anti-imaging filter – Changing the sampling rate by rational factors</td>
<td>5</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Transposition theorem-Multirate identities - Direct and Transposed FIR structures for interpolation and decimation filters – The Polyphase decomposition - Polyphase implementation of decimation and interpolation filters. Commutator models - Multistage implementation of sampling rate conversion – Filter requirements for multistage designs – Overall and individual filter requirements.</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
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</tr>
<tr>
<td>MODULE 4: Tree structured filter banks-Applications of multirate systems in communication-Timing Recovery in a digital demodulator, Modern carrier recovery, FM band channelizer. Short time Fourier Transform and Wavelets: Filtering interpretation of STFT – Filter bank implementation - Time frequency resolution trade off – Sampling of STFT in time and frequency</td>
<td>6</td>
<td>15</td>
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<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
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END SEMESTER EXAM
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
--- | --- | --- | ---
04 EC 6204 | MIXED SIGNAL CIRCUIT DESIGN | 3-0-0: 3 | 2015

Pre-requisites: Nil

Course objectives

- To introduce to MOS models
- To give insight in to the design of opamp
- To analyze and design switched capacitor circuits, DAC & ADC

Syllabus

CMOS Technology - device modeling - CMOS amplifier - Design of CMOS Op Amp: - PSSR – comparators - Switched Capacitor Circuits - Z domain model - ADC and DAC – PLL - Sense amplifiers

Course Outcome:

Students finishing this course will have the ability

- to understand and analyze MOS models
- to design opamp based circuits
- to analyze and design switched capacitor circuits, DAC & ADC

Text book


References

<table>
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<th>COURSE CODE:</th>
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<tr>
<td>04 EC 6204</td>
<td>Mixed Signal Circuit Design</td>
<td>3 -0-0: 3</td>
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</table>

**MODULES**

<table>
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<tr>
<th>MODULE 1: CMOS Technology</th>
<th>Basic MOS semiconductor fabrication process. MOS transistors. CMOS device modelling, Small signal model for MOS transistors. Computer simulation model. Subthreshold MOS model</th>
<th>8</th>
<th>15</th>
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</thead>
<tbody>
<tr>
<td>MODULE 2: CMOS amplifier</td>
<td>Differential amplifier, Cascode amplifier. Current amplifier, Output amplifiers. High gain amplifier architecture.</td>
<td>6</td>
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**INTERNAL TEST 1 (MODULE 1 & 2)**

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<tr>
<th>MODULE 3: Design of CMOS Op Amp</th>
<th>Compensation. Design of two stage op amp. PSSR of two stage opamp. Cascode op amp. Buffered op amp</th>
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<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 4: High speed or frequency op amp, micro power op amp, Low noise op amp, Low voltage op amp</td>
<td>Design of two stage open loop comparators. High speed comparators</td>
<td>7</td>
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</table>

**INTERNAL TEST 2 (MODULE 3 & 4)**

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<tr>
<th>MODULE 5: Switched Capacitor Circuits</th>
<th>Switched capacitor amplifiers. Switched capacitor integrators. Z domain model of two phase switched capacitor. First order switched capacitor circuits, second order switched capacitor circuits. Switched capacitor filters</th>
<th>7</th>
<th>20</th>
</tr>
</thead>
</table>

**END SEMESTER EXAM**
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
--- | --- | --- | ---
04 EC 6206 | SYSTEM DESIGN USING ARM | 3-0-0:3 | 2015

Pre-requisites: Nil

Course Objectives:

To give the Student:-

- To provide an introduction about embedded system and ARM processors
- To understand instruction sets and assembly language programming of ARM
- To understand architectural support for high level languages and memory

Syllabus

General system design, ARM architecture and programming, ARM Instruction Set, Architectural support and memory, Memory hierarchy

Course Outcome:

Use of ARM architecture and programming concepts into design process

Students who successfully understand ARM instruction set, memory architecture and hierarchy

Text book

1. ARM System-on-chip architecture, Steve Furber, Pearson Education

Reference:

2. Computers as Components-principles of Embedded computer system design, Wayne Wolf, Elsevier
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<tr>
<td>04 EC 6206</td>
<td>SYSTEM DESIGN USING ARM</td>
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<th>MODULES</th>
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<th>Sem. Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: General system design</td>
<td>6</td>
<td>15</td>
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<tr>
<td>MODULE 2: ARM architecture and programming</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>Overview of ARM architecture – Architecture inheritance, Programmer’s model, Development tools. ARM assembly language programming</td>
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<tr>
<td>MODULE 3: ARM Instruction Set</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>ARM organization and implementation. ARM instruction set (exceptions, conditional execution, branching instructions, multiply instructions, coprocessor instructions).</td>
<td></td>
<td></td>
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<tr>
<td>MODULE 4: Instruction Sets</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>Data types, Floating point datatypes, Conditional statements, Loops, Use of memory, Run-time environment environment. Thumb instruction set-Thumb bit, Thumb programmer’s model, Thumb branch instructions, Thumb software interrupt instructions</td>
<td></td>
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</tr>
<tr>
<td>MODULE 5: Architectural support and memory</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>Architectural support for system development- ARM memory interface, AMBA, ARM reference peripheral specifications, H/w system prototyping tools, ARMuLator, JTAG, ARM debug architecture, Embedded trace, signal processing support, ARM processor cores. Memory size and speed, On-chip memory, Caches, Memory management.</td>
<td></td>
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<tr>
<td>MODULE 6: Memory hierarchy</td>
<td>7</td>
<td>20</td>
</tr>
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</table>

END SEMESTER EXAM
Pre-requisites: Nil

Objectives:

- To provide an overview of wireless channel characteristics
- To understand the basic concepts of synchronization and channel estimation
- To evaluate its performance and discuss different channel optimization techniques

Syllabus


Course Outcome:

Students finishing this course will have the ability

- to understand and analyze MOS models
- to design op-amp based circuits
- to analyse and design switched capacitor circuits, DAC & ADC

Text book


References:

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<td>04 EC 6108</td>
<td>MULTI CARRIER COMMUNICATION SYSTEMS</td>
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<th>MODULES</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tr>
<td>MODULE 1: Review of wireless channel characteristics - Multi carrier and OFDM system fundamentals - OFDM system model - Comparison with single carrier - Channel capacity and OFDM</td>
<td>8</td>
<td>15</td>
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<tr>
<td>MODULE 2: FFT implementation - Power spectrum - Impairments of wireless channels to OFDM signals - Comparison with other multicarrier modulation scheme: MC CDMA</td>
<td>6</td>
<td>15</td>
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<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
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</tr>
<tr>
<td>MODULE 3: Synchronization in OFDM - Timing and Frequency Offset in OFDM, Synchronization &amp; system architecture, Timing and Frequency Offset estimation - Pilot and Non pilot based methods, Joint Time &amp; Frequency Offset estimation.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Channel Estimation in OFDM systems - Differential and Coherent detection; Pilot symbol aided estimation - Block type and Comb type pilot arrangement; Decision directed channel estimation</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
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<td></td>
</tr>
<tr>
<td>MODULE 5: MMSE estimation using time and frequency domain correlation; MIMO channel estimation- basic concepts; Concepts of Time and Frequency domain equalization.</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>MODULE 6: Clipping in Multi carrier systems - Power amplifier non linearity - Error probability analysis - Performance in AWGN. PAPR properties of OFDM signals - PAPR reduction techniques with signal distortion; Techniques for distortion less PAPR reduction - Selective mapping and Optimization techniques</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>END SEMESTER EXAM</td>
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</tbody>
</table>
Pre-requisites: Nil

Course objectives

- To learn human speech production mechanism and different categorization of sounds
- To learn various speech analysis techniques
- To study features and modeling techniques for speech recognition
- To understand the fundamentals of speech coding, synthesis and enhancement

Syllabus

Speech Production and Categorization of Speech Sounds - Introduction to speech signal processing – applications - human speech production mechanism - Speech Analysis - Time and frequency domain analysis, Review of DSP techniques-z-transform, Discrete Fourier transform - Speech Recognition - mel frequency cepstral coefficient(MFCC), dynamic time warping(DTW), Gaussian mixture models (GMM), hidden Markov model(HMM), speaker and language recognition. Speech Coding, Speech Synthesis and Enhancement

Course Outcome:

Students finishing this course will have the ability

- To Categorize of Speech Sounds
- To analyse speech recognition models
- To analyse and model Speech Synthesis and Enhancement

Text Books:


References:

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<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 EC 6114</td>
<td>Speech Technology</td>
<td>3-0-0:3</td>
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**MODULES**

<table>
<thead>
<tr>
<th>MODULE</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tbody>
<tr>
<td>1:</td>
<td></td>
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</tr>
<tr>
<td>Speech Production and Categorization of Speech Sounds - Introduction to speech signal processing, overview of speech signal processing applications, human speech production mechanism, Acoustic theory of speech production, nature of speech signal, spectrographic analysis of speech, categorization of speech sounds, co-articulation, prosody</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>2:</td>
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<tr>
<td>Speech Analysis - Time and frequency domain analysis, Review of DSP techniques-z-transform, Discrete Fourier transform, short-time analysis of speech, linear prediction analysis, cepstral analysis</td>
<td>6</td>
<td>15</td>
</tr>
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</table>

**INTERNAL TEST 1 (MODULE 1 & 2)**

<table>
<thead>
<tr>
<th>MODULE</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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</thead>
<tbody>
<tr>
<td>3:</td>
<td></td>
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<tr>
<td>Contrasting linear prediction analysis and cepstral analysis, vector quantization(VQ) methods.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>4:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Speech recognition, Bayes rule, segmental feature extraction, mel frequency cepstral coefficient(MFCC), dynamic time –warping(DTW)</td>
<td>7</td>
<td>15</td>
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</tbody>
</table>

**INTERNAL TEST 2 (MODULE 3 & 4)**

<table>
<thead>
<tr>
<th>MODULE</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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</thead>
<tbody>
<tr>
<td>5:</td>
<td></td>
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<tr>
<td>Gaussian mixture models (GMM), hidden Markov model(HMM), approaches for speech, speaker and language recognition</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>6:</td>
<td></td>
<td></td>
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<tr>
<td>Speech coding, time-domain waveform coding, Linear predictive coding, CELP coding. Principles of speech synthesis, fundamentals of speech enhancement Radios. Spectrum Sensing to Detect Specific Primary System</td>
<td>7</td>
<td>20</td>
</tr>
</tbody>
</table>

**END SEMESTER EXAM**
Pre-requisites: Nil

Course Objectives:

- To study algorithms and parallel processing
- To understand various DSP architectures and filters
- To provide an insight into Pipelining of recursive filters

Syllabus

Review of DSP algorithms - DSP algorithm Representation - Iteration Bound - Loop Bound - Pipelining and Parallel Processing for FIR filters - Pipelining and Parallel Processing for low power - Retiming Techniques - Unfolding algorithm - Folding - Transformations - Systolic DSP architecture design - fast convolution algorithms

Course Outcome:

Students finishing this course will have the ability

- To apply pipelining and parallel processing techniques for performance enhancement
- To analysed data flow graphs for retiming, folding and unfolding
- To perform fast convolution operations

Textbook


References:

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<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<tr>
<td>04 EC 6208</td>
<td>VLSI SIGNAL PROCESSING</td>
<td>3-0-0:3</td>
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**MODULES**

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<thead>
<tr>
<th>Modules</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: Review of DSP algorithms, Iteration Bound, Loop Bound, Iteration Bound Algorithms, Iteration Bound for multirate data flow graphs.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Pipelining and Parallel Processing: Introduction, pipelining and parallel processing of FIR filters pipelining and parallel processing for low power</td>
<td>6</td>
<td>15</td>
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**INTERNAL TEST 1 (MODULE 1 & 2)**

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<tr>
<th>Modules</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 3: Retiming-introduction, properties, system inequalities, retiming techniques- cutset retiming and pipelining, retiming for clock period minimisation</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Unfolding: Introduction, unfolding algorithm, properties, critical path unfolding and retiming, applications- sample period reduction, parallel processing- 3-unfold and 3-parallel examples</td>
<td>7</td>
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**INTERNAL TEST 2 (MODULE 3 & 4)**

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<tr>
<th>Modules</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 5: Folding: Introduction, Transformation, register minimization techniques- life time analysis, data allocation using forward-backward register allocation folding of multi rate systems</td>
<td>7</td>
<td>20</td>
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</tbody>
</table>

**END SEMESTER EXAM**
Pre-requisites: Nil

Course Objectives:

To give the Student:-

- To learn about the concepts and principles of mobile computing;
- To explore both theoretical and practical issues of mobile computing;
- To develop skills of finding solutions and building software for mobile computing applications.

Syllabus


Course Outcome:

Grasp the concepts and features of mobile computing technologies and applications. The student have a good understanding of how the underlying wireless and mobile communication networks work, their technical features, and what kinds of applications they can support. He could identify the important issues of developing mobile computing systems and applications.

Text Books:


References:


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<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
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<tbody>
<tr>
<td>04 EC 6212</td>
<td>Mobile Computing</td>
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<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: Mobile Computing (MC): Motivations, concepts, challenges, and applications of mobile computing; relationship with distributed computing, Internet computing, ubiquitous/pervasive computing. Mobile computing models and architectures.</td>
<td>8</td>
<td>15</td>
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| INTERNAL TEST 1 (MODULE 1 & 2) | 8 | 15 |

| MODULE 3: GSM: Mobile services, System architecture, Radio interface, Protocols, Localization and calling, Handover, Security, and New data services. Motivation for a specialized MAC (Hidden and exposed terminals, Near and far terminals) | 8 | 15 |

| MODULE 4: Mobile IP (Goals, assumptions, entities and terminology, IP packet delivery, agent advertisement and discovery, registration, tunneling and encapsulation, optimizations) Dynamic Host Configuration Protocol (DHCP). Traditional TCP, Indirect TCP, Snooping TCP Mobile TCP, Fast retransmit/fast recovery, Transmission /time-out freezing, Selective retransmission, Transaction oriented TCP. | 8 | 15 |

| INTERNAL TEST 2 (MODULE 3 & 4) | 5 | 20 |

| MODULE 5: Hoarding techniques, caching invalidation mechanisms, client server computing with adaptation, power-aware and context-aware computing Transactional models, query processing, recovery, and quality of service issues | 5 | 20 |

| MODULE 6: Communications asymmetry, classification of new data delivery mechanisms, push-based mechanisms. Pull-based mechanisms, hybrid mechanisms, selective tuning (indexing) techniques | 5 | 20 |

| END SEMESTER EXAM | | |
Pre-requisites: Nil

Objectives

Upon completing the course, the student will:

- be familiar with the basics of MIMO communication;
- be familiar with various Diversity and Multiplexing techniques of MIMO;
- be exposed to Space Time Block Codes;

Syllabus

Theoretic aspects of MIMO: Review of SISO fading communication channels, MIMO channel models - MIMO Diversity and Spatial multiplexing - Space time receivers - Space Time Block Codes - Performance analysis - Space Time Trellis Codes - Delay diversity - Performance analysis.

Course Outcome:

Students finishing this course will have the ability

- To model MIMO channels
- To analyse Diversity and Multiplexing techniques of MIMO
- To analyse space time block codes

Text books


References:


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<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<td>04 EC 6116</td>
<td>MIMO Communication Systems</td>
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<th>MODULES</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: Review of SISO fading communication channels, MIMO channel models, Classical i.i.d. and extended channels. Frequency selective and correlated channel models, Capacity of MIMO channels</td>
<td>8</td>
<td>15</td>
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<tr>
<td>MODULE 2: Ergodic and outage capacity, Capacity bounds and Influence of channel properties on the capacity.</td>
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<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 3: MIMO Diversity and Spatial Multiplexing- Sources and types of diversity, analysis under Rayleigh fading, Diversity and channel knowledge. Alamouti space time code, MIMO spatial multiplexing. Space time receivers</td>
<td>7</td>
<td>15</td>
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<tr>
<td>MODULE 4: ML, ZF, MMSE and Sphere decoding, BLAST receivers and Diversity multiplexing trade-off.Space time block codes on real and complex orthogonal designs, Code design criteria for quasi-static channels (Rank, determinant and Euclidean distance)</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td>7</td>
<td>20</td>
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<tr>
<td>MODULE 5: Orthogonal designs, Generalized orthogonal designs, Quasi-orthogonal designs and Performance analysis.</td>
<td>7</td>
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<tr>
<td>MODULE 6: Representation of Space Time Trellis Codes, shift register, generator matrix, state-transition diagram, trellis diagram.Code construction, Delay diversity as a special case of STTC and Performance analysis.</td>
<td>7</td>
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</tbody>
</table>

END SEMESTER EXAM
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
--- | --- | --- | ---
04 EC 6214 | Nano Electronics | 3 -0-0: 3 | 2015

Pre-requisites: Nil

Course Objectives:

To give the Student:-

- To learn and understand basic and advance concepts of Nano electronics.

Syllabus

Basics of Nanoelectronics, Basics of lithographic techniques for Nano electronics, Quantum electron devices, Nanoelectronics with tunneling devices and superconducting devices, Principles of Single Electron Transistor (SET), Nano designs and Nanocontacts, A survey about the limits, Limits due to thermal particle motion Memory devices and sensors, Ferroelectric thin film properties and integration gas sensitive FETs

Course Outcome:

The students should be able to understand basic and advanced concepts of nanoelectronic devices, sensors and transducers and their applications in nanotechnology.

Text Books:


References:

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<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<tr>
<td>04 EC 6214</td>
<td>Nano Electronics</td>
<td>3-0-0:3</td>
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**MODULES**

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<tr>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tr>
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<td>15</td>
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</table>

**MODULE 1:** Basics of Nanoelectronics – capabilities of Nanoelectronics – physical fundamentals of Nanoelectronics – basics of information theory – the tools for micro and nano fabrication – basics of lithographic techniques for Nanoelectronics.


**INTERNAL TEST 1 (MODULE 1 & 2)**

<table>
<thead>
<tr>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
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<td>15</td>
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</table>


**MODULE 4:** Molecular electronics – elementary circuits – flux quantum devices – application of superconducting devices – Nanotubes based sensors, fluid flow, gas temperature; Strain –oxide nanowire, gas sensing (ZnO,TiO2,SnO2,WO3), LPG sensor (SnO2 powder)- Nano designs and Nanocontacts – metallic nanostructures

**INTERNAL TEST 2 (MODULE 3 & 4)**

<table>
<thead>
<tr>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<td>15</td>
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</table>

**MODULE 5:** A survey about the limits – Replacement Technologies – Energy and Heat dissipation – Parameter spread as Limiting Effect – Limits due to thermal particle motion – Reliability as limiting factor – Physical limits – Final objectives of integrated chip and systems


**END SEMESTER EXAM**
Pre-requisites: Nil

Objectives:

- To learn the various techniques pertaining to linear and nonlinear optimization problems
- To be introduced to graph theory and combinatorial optimization.

Syllabus

Unconstrained optimization - one dimensional search methods - gradient methods - Linear Programming - Convex polyhedral - Simplex algorithm - Matrix form of the simplex algorithm - non simplex methods - Nonlinear Constrained Optimization: - Introduction to Graph Theory and Combinatorial Optimization

Course Outcome:

Students finishing this course will have the ability

- To apply the concepts of optimization to specific engineering problems
- To analyse problems based on graph theory and combinatorial optimization

Text books

1. Edwin K. P. Chong, Stanislaw H. ZAK, An Introduction to Optimization, 2nd Ed, John Wiley & Sons

References

2. Jonathan L Grosss, Jay Yellen, Chapmann and Hall, Graph theory and its application, 2e, CRC pub,
3. Alan Tucker, Applied Combinatorics, John Wiley and Sons
4. Dimitri P. Bertsekas, Nonlinear programming, Athena Scientific
<table>
<thead>
<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 EC 6122</td>
<td>Optimization Techniques</td>
<td>3-0-0:3</td>
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<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: Unconstrained optimization- Necessary and sufficient conditions for local minima, one dimensional search methods, gradient methods, steepest descent, Inverse Hessian</td>
<td>8</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Newton’s method, conjugate direction method, conjugate gradient algorithm, quasi Newton methods</td>
<td>7</td>
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<tr>
<th>INTERNAL TEST 1 (MODULE 1 &amp; 2)</th>
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<tbody>
<tr>
<td>MODULE 3: Linear Programming- Convex polyhedra, standard form of linear programming, Basic solutions, Simplex algorithm. Matrix form of the simplex algorithm, Duality, non simplex methods: Khachiyan method, Karmarkar’s method</td>
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<tbody>
<tr>
<td>MODULE 5: Introduction to Graph Theory and Combinatorial OptimizationRouting-traveling salesman; Assignment – satisfiabilty, constraint satisfiability, graph coloring</td>
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<tr>
<td>MODULE 6: Subsets- set covering, partitioning; Scheduling; Shortest path and Critical path algorithms</td>
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<th>END SEMESTER EXAM</th>
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</table>
Course Code: 04 EC 6216  
Course Name: Optical Networks And Systems  
L-T-P-C: 3-0-0: 3  
Year: 2015

Pre-requisites: Nil

Course Objectives:

To give the Student:-

- A basis in unguided optical communication system, integrated optics and optical switches;
- A foundation about digital transmission systems;
- A guide to design different multiplexing schemes;
- An overview to Soliton Systems;

Syllabus

Unguided optical communication system, integrated optics, active and passive components, opto-mechanical switches, all optical switches, digital transmission systems, transmission distance for single mode link line coding, NRZ codes, RZ codes, block codes, multiplexing schemes, fiber grating filters, Tunable filters, system consideration and tunable filter types, optical amplifiers, optical networks, SONET/SDH, transmission formats and speeds, optical interfaces, SONET/SDH rings, SONET/SDH networks, Nonlinear effects on network performance, Solitons, Optical CDMA, Ultra high capacity networks.

Course Outcome:

Students finishing this course will have the ability to be familiar with unguided optical communication system; Use the passive and active components; realize the use of optical switches; Understand the use of different optical amplifier for different purpose; Use the solitons in an apt manner.

Text Books:


References:

<table>
<thead>
<tr>
<th>COURSE CODE: 04 EC 6216</th>
<th>COURSE TITLE: Optical Networks And Systems</th>
<th>CREDITS 3-0-0:3</th>
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**MODULES**

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<tr>
<th>MODULE</th>
<th>CONTACT HOURS</th>
<th>SEM. EXAM MARKS (%)</th>
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<tbody>
<tr>
<td>1: Unguided optical communication system: transmission parameters, beam divergence, atmospheric attenuation, guided wave communication, merits of optical fibre communication systems, basic network information rates, time evolution of fibre optic systems, elements of optical fiber transmission link/repeaters</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>2: Integrated optics, active and passive components, opto-mechanical switches, parameter of optical switches, optical Packet Switch, optical Burst Switch and all optical switches.</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>3: Digital transmission systems: Point to point links, system considerations, link power budget, rise-time budget, first window transmission distance, transmission distance for single mode link line coding, NRZ codes, RZ codes, block codes</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>4: Coherent systems, homodyne and heterodyne detection. Multiplexing schemes, TDM, WDM concepts and components, operational principles of WDM, passive components, 2 x 2 fibre coupler, fiber grating filters, Tunable filters, system consideration and tunable filter types.</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>5: Optical amplifiers: general applications and amplifier types, semiconductor optical amplifiers, external pumping, amplifier gain, erbium doped fiber amplifiers, amplification mechanism, EDFA architecture, EDFA power conversion efficiency and gain, amplifier noise.</td>
<td>6</td>
<td>20</td>
</tr>
<tr>
<td>6: Optical networks: network topologies, performance of passive linear buses, performance of star architectures, SONET/SDH, transmission formats and speeds, optical interfaces, SONET/SDH rings, SONET/SDH networks, Nonlinear effects on network performance, Solitons, Optical CDMA, Ultra high capacity networks.</td>
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END SEMESTER EXAM
Each student shall prepare a seminar paper on any topic of interest related to the core/elective courses being undergone in the second semester of the M.Tech programme. He/she shall select paper from IEEE/other reputed international journals. They should get the paper approved by the Programme Coordinator/Faculty Members in the concerned area of specialization and shall present it in the class in the presence of Faculty in-charge of seminar class. Every student shall participate in the seminar. Grade will be awarded on the basis of the student’s paper, presentation and his/her participation in the seminar.

Goals: This course is designed to improve written and oral presentation skills and to develop confidence in making public presentations, to provide feedback on the quality and appropriateness of the work experience, and to promote discussions on design problems or new developments.
Pre-requisites: Nil

Objectives:
- To develop an idea about the basic combinational logic programming.
- To program sequential logic, memories and state machines
- To design systems using FPGA and CPLD

Modeling and Functional Simulation of the following digital circuits (with Xilinx/ModelSim tools) using Verilog Hardware Description Languages

1. Part – I
   Combinational Logic: Basic Gates, Multiplexer, Comparator, Adder/ Subtractor, Multipliers, Decoders, Address decoders, parity generator, ALU

2. Part – II

3. Part – III
   Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs

4. Part-IV:
   FPGA System Design: Demonstration of FPGA and CPLD Boards, Demonstration of Digital design using FPGAs and CPLDs. Implementation of UART/Mini Processors on FPGA/CPLD

*** Programming can be done using any compiler. Download the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.
SEMESTER III
ELECTIVE IV

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<th>L-T-P:C</th>
<th>YEAR</th>
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<tbody>
<tr>
<td>04 EC 7201</td>
<td>DESIGN OF ASIC</td>
<td>3-0-0:3</td>
<td>2015</td>
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</table>

Pre-requisites: Nil

Objectives

- To study various types of ASICs and FPGAs
- To provide an insight into synchronous Design Using Programmable Devices
- To study System Design Using Verilog HDL

Syllabus

Introduction to ASICs - Types of ASICs - PLD – FPGA - Logical effort - Programmable ASICS, Programmable ASIC Logic cells: Anti fuse, static RAM, EPROM and EEPROM technology - PREP benchmarks – examples of Actel, Xilinx Altera FPGA architectures- Synchronous Design Using Programmable Devices- System Design Using Verilog HDL -Modelling hardware units using Verilog

Course Outcome:

Students finishing this course will have the ability

- To properly select programmable logic devices for various applications
- To analyse data flow graphs for retiming, folding and unfolding
- To analyse Verilog modeling of hardware

Text books


References:

3. Cyclone III Device Hand book, Volume 1
<table>
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<tr>
<th>COURSE CODE:</th>
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<tr>
<td>04 EC 7201</td>
<td>DESIGN OF ASIC</td>
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<tr>
<td>Contact Hours</td>
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<tr>
<td>MODULE 1: Introduction to ASICs, Types of ASICs, full custom ASIC,</td>
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<td>MODULE 2: Programmable ASIC, PLD, FPGA, Logical effort, Programmable</td>
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<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
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<tr>
<td>MODULE 3: Actel ACT, Xilinx LCA, Altera FLEX, Altera MAX, Architecture</td>
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<td>MODULE 4: Synchronous Design Using Programmable Devices, EPROM to</td>
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<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
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<tr>
<td>MODULE 5: System Design Using Verilog HDL, Verilog Description of</td>
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<tr>
<td>MODULE 6: Modelling using Verilog, Flip Flops, registers, counters,</td>
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END SEMESTER EXAM
Pre-requisites: VLSI Signal processing

Course objective

- To have an understanding about the pipelining used in FIR and IIR filters.
- To understand the designing and features of parallel FIR filter
- To learn about the characteristic features of a IIR filter
- Basic knowledge about DSP processors used in various communication systems

Syllabus


Course Outcome:

Students finishing this course will have the ability

- To apply pipelining and parallel processing techniques for performance enhancement on IIR and adaptive systems
- To analyse scaling and round-off noise in IIR filters
- To analyse the features of DSP processors used in various applications

Text books


References

1 .Uwemeyer-Baes, DSP with Field programmable gate arrays, Springer, 2001
<table>
<thead>
<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE:</th>
<th>CREDITS:</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 EC 7203</td>
<td>VLSI Structures For DSP</td>
<td>3-0-0:3</td>
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</table>

<table>
<thead>
<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULE 1: Review of Pipelining and parallel processing for FIR filters, algorithmic strength reduction-introduction, parallel FIR filters, Discrete Cosine Transform and inverse DCT</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 2: Discrete time cosine transform – implementation of DCT and inverse DCT based on algorithm-architecture transformations – parallel architectures for rank order filters.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 1 (MODULE 1 &amp; 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODULE 3: Pipelining in IIR filters – parallel processing for IIR filters – combined pipelining and parallel processing of IIR filters.</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>MODULE 4: Low power IIR filter design, Pipelined adaptive digital filters - rlsxed look ahead - product, sum and delay look ahead</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MODULE 5: Scaling and round off noise - Round off noise in pipelined IIR filters – round off noise in lattice filters, pipelining of lattice IIR digital filters – low power CMOS lattice IIR filters</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>MODULE 6: Evolution of programmable DSP processors – DSP processors for mobile and wireless communications, processors for multimedia signal processing – FPGA implementation of DSP processors</td>
<td>7</td>
<td>20</td>
</tr>
</tbody>
</table>

END SEMESTER EXAM
Pre-requisites: Nil

Course Objectives:

- To provide an insight into hazards in combinational circuits
- To understand design and analysis of synchronous and asynchronous state machines
- To understand ASM and its design

Syllabus

Propagation delay and timing defects in combinational logic - hazards types and characteristics -
Synchronous state machine design and analysis - output race glitches, detection and elimination of
static hazards in the output logic, asynchronous inputs - clock skew, clock sources and clock signal
specifications – FSM – design of controller, data path and functional partition. - Asynchronous state
machine design and analysis - LPD model - Rendezvous modules - timing defects in asynchronous FSMs-
Design using Algorithmic State Machines (ASM) chart

Course Outcome:

Students finishing this course will have the ability

- To analyse timing hazards
- To design and analyse synchronous and asynchronous state machines
- To design systems using ASM

Text books


References:

<table>
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<tr>
<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
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</thead>
<tbody>
<tr>
<td>04 EC 7205</td>
<td>Advanced Digital System Design Techniques</td>
<td>3-0-0:3</td>
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</table>

**MODULES**

<table>
<thead>
<tr>
<th>MODULE</th>
<th>Description</th>
<th>Contact Hours</th>
<th>Exam Marks (%)</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>Hazards – static and dynamic, essential hazards, static hazard free and dynamic hazard free combinational logic circuits design, functional hazards</td>
<td>8</td>
<td>15</td>
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<tr>
<td>2</td>
<td>Direct digital synthesizers, CORDIC algorithm, Pulse shaping and interpolation filters, DDS with tunable DSM, Transmitter and receiver architectures</td>
<td>6</td>
<td>15</td>
</tr>
<tr>
<td>3</td>
<td>Design of simple synchronous state machine design with edge-triggered flip-flop, analysis of simple state machine, detection and elimination of output race glitches, detection and elimination of static hazards in the output logic</td>
<td>7</td>
<td>15</td>
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<tr>
<td>4</td>
<td>Asynchronous inputs: rules and caveats, clock skew, clock sources and clock signal specifications, initialization and reset of the FSM: sanity circuits, design of complex state machines, algorithmic state machine charts and state tables, array algebraic approach to logic design, state minimization, system-level design: controller, data path and functional partition</td>
<td>7</td>
<td>15</td>
</tr>
<tr>
<td>5</td>
<td>Lumped path delay models for asynchronous FSMs, functional relationships and stability criteria, excitation table for LPD model, state diagram, K maps and state table for asynchronous FSMs, Design of the basic cells by using the LPD model, design of the Rendezvous modules, RET D flip-flop, RET JK flip-flop.</td>
<td>7</td>
<td>20</td>
</tr>
<tr>
<td>6</td>
<td>Detection and elimination of timing defects in asynchronous FSMs, single-transition-timemachines and array algebraic approach, hazard-free design of fundamental mode FSMs, One-hot design of asynchronous state machines, Design and analysis of fundamental mode FSMs, Design of state machines using Algorithmic State Machines (ASM) chart as a design tool.</td>
<td>7</td>
<td>20</td>
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</table>

**INTERNAL TEST 1 (MODULE 1 & 2)**

**INTERNAL TEST 2 (MODULE 3 & 4)**

**END SEMESTER EXAM**
Pre-requisites: Nil

Objective:

- To develop a good understanding of the various pattern recognition techniques and its applications

Syllabus


Course Outcome:

Students finishing this course will have the ability

- To understand feature vectors and classifiers
- To design and analyse pattern classification problems

Text books


References:

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<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
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<tr>
<td>04 EC 7207</td>
<td>Pattern Recognition</td>
<td>3 -0-0: 3</td>
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<tr>
<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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</table>

| MODULE 1: Features, feature vectors and classifiers, Supervised versus unsupervised pattern recognition. Classifiers based on Bayes' Decision theory-introduction, discriminant functions and decision surfaces | 8 | 15 |

| MODULE 2: Bayesian classification for normal distributions, Estimation of unknown probability density functions, the nearest neighbour rule. Linear classifiers, Linear discriminant functions and decision hyper planes, The perceptron algorithm | 6 | 15 |

<table>
<thead>
<tr>
<th>INTERNAL TEST 1 (MODULE 1 &amp; 2)</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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</table>

| MODULE 3: Gaussian mixture models, expectation maximization, pattern classification problems – linear and nonlinear multilayer feed forward neural networks, back propagation algorithm, Radial basis function networks. | 7 | 15 |

| MODULE 4: Support Vector machines-nonlinear case, decision trees, combining classifiers, feature selection, Receiver Operating Characteristics (ROC) curve | 7 | 15 |

<table>
<thead>
<tr>
<th>INTERNAL TEST 2 (MODULE 3 &amp; 4)</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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</table>

| MODULE 5: Class separability measures, optimal feature generation, the Bayesian information criterion, dimension reduction technique: PCA, FDA. | 7 | 20 |

| MODULE 6: Cluster analysis, proximity measures, clustering algorithms - sequential algorithms machine. Hierarchical algorithms - agglomerative algorithms, divisive algorithms, K-means algorithm | 7 | 20 |

| END SEMESTER EXAM | Contact Hours | Sem. Exam Marks (%) |
Course Objectives:

- To provide an insight into the static and dynamic cmos logic
- To understand and design cmos adders, multipliers and control unit
- To understand Designing of memory and array structures

Syllabus

Static and Dynamic design - Logic efforts -tristate inverter and CMOS logic gates - Layout-examples - Fundamentals of dynamic logic: High performance dynamic circuits-Domino – TSPC - Pass transistor and transmission gate logic –SOI - Data path sub systems – design of adder and shifter - parity generator-ALU design- FSM and PLA based design - design of multipliersDesigning of memory – SRAM - DRAM - Multi-Ported memory -Subarray Architectures - Embedded DRAM - Read-Only Memory: Content-Addressable Memory: Programmable Logic Arrays, Robust Memory Design

Course Outcome:

Students finishing this course will have the ability

- To distinguish between various types of CMOS logic devices
- To design CMOS based datapath and control units
- To analyse various CMOS based memory types

Text books


References:

2. C.Mead and L.Coway, “Introduction to VLSI systems”, Addison Wesley, 1999
4. S.Srinivasan, “VLSI Circuits”, NPTEL Courseware, 2005
<table>
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<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
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<tbody>
<tr>
<td>04 EC 7209</td>
<td>VLSI Subsystem Design</td>
<td>3 -0:0:3</td>
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<th>MODULES</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
<tr>
<td>MODULE 1: Tristate inverter, static CMOS logic gates, properties(2 input NAND, NOR), Logic efforts, Combinational logic circuits- Layout-examples; Fundamentals of dynamic logic: High performance dynamic circuits-Domino CMOS</td>
<td>8</td>
<td>15</td>
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<tr>
<td>MODULE 2: Multi Output Domino Logic, Dual-rail Domino Logic, NP Domino logic(NORA), True-Single-Phase-Clock(TSPC) CMOS logic; Pass transistor and transmission gate logic, examples. Silicon-On-Insulator Circuit Design: Floating Body Voltage, SOI Advantages, Disadvantages</td>
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<th>INTERNAL TEST 1 (MODULE 1 &amp; 2)</th>
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<tr>
<td>INTERNAL TEST 2 (MODULE 3 &amp; 4)</td>
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</table>

| MODULE 3: Design of adders: bit parallel, bit serial, carry look ahead adder, multi level circuits, carry save and carry skip adders, conditional sum adder, one/zero detector, magnitude comparator, Counters- binary, LFSR; parity generator; Shifters: Funnel shifter, Barrel shifter, Datapath design case study | 7             | 15                  |
| MODULE 4: ALU design- design of multipliers: parallel multipliers, array, 2’s complement, Booth, Braun, Baugh-Wooley, Wallace tree, Dadda multipliers; serial multiplier. Design of control unit: FSM design procedure, PLA based design. | 8             | 15                  |

| MODULE 5: SRAM: SRAM Cells, Row Circuitry, Column Circuitry, Multi-Ported SRAM; DRAM: Subarray Architectures, Column Circuitry, Embedded DRAM; Read-Only Memory: Programmable ROMs, NAND ROMs; Flash Serial Access Memories: Shift Registers, Queues (FIFO, LIFO), Content-Addressable Memory | 7             | 20                  |
| MODULE 6: Programmable Logic Arrays, Robust Memory Design: Redundancy, Error Correcting Codes (ECC), Memory reliability and yield, Power dissipation in memories. Memory design:-case study | 6             | 20                  |

END SEMESTER EXAM
Pre-requisites: Nil

Course Objectives:

• To provide an introduction about VLSI testing
• To understand logic simulation and test designs
• To study various memory tests

Syllabus


Course Outcome:

Students finishing this course will have the ability

• To understand various VLSI testing procedures
• to design for fault modeling and logic simulation
• to analyse various types of VLSI testing

Text book


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<tbody>
<tr>
<td>04 EC 7211</td>
<td>Testing Of VLSI Circuits</td>
<td>3 -0-0: 3</td>
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### MODULES

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<th>Modules</th>
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<th>Sem. Exam Marks (%)</th>
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**MODULE 1: VLSI testing process and Test Equipment, Test Economics and Product Quality, why fault modeling, Fault Modeling**

7 hours of contact hours, 15% exam marks

**MODULE 2: Logic and Fault Simulation, glossary of Faults, single stuck-at-faults, functional equivalence, bridging faults.**

7 hours of contact hours, 15% exam marks

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**INTERNAL TEST 1 (MODULE 1 & 2)**

**MODULE 3: Modeling single states, algorithm for true value simulation, serial and parallel fault simulation, Testability Measures, Combinational Circuit Test Generation, Sequential Circuit Test Generation**

7 hours of contact hours, 15% exam marks

**MODULE 4: Digital DFT and Scan design, Built-in Self test, Random logic BIST and memory logic BIST, Boundary Scan standard**

7 hours of contact hours, 15% exam marks

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**INTERNAL TEST 2 (MODULE 3 & 4)**

**MODULE 5: Analog and Mixed signal Test, delay test, IDDQ Test, DFT Fundamentals, ATPQ Fundamental**

7 hours of contact hours, 20% exam marks

**MODULE 6: Scan Architecture and Technique, System Test, Embedded Core Test, Future Testing.**

7 hours of contact hours, 20% exam marks

---

**END SEMESTER EXAM**
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
---|---|---|---
04 EC 7213 | ADVANCED DIGITAL COMMUNICATION | 3-0-0:3 | 2015

Pre-requisites: Nil

Objectives:
- To characterize the communication systems
- To learn various digital modulation schemes
- To study optimum receivers for AWGN channel
- To learn communication through bandlimited channels

Syllabus


Course Outcome:

Students finishing this course will have the ability
- to model various types of communication system
- to design transmitters and receivers for communication schemes with different modulation techniques
- to deal with ISI
- to analyse various types of channels and signals

Text book


References:

1. Bruce Carlson, Crilly&Rutledge, Communication systems, McGraw Hill
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<tr>
<th>COURSE CODE:</th>
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<tbody>
<tr>
<td>04 EC 7213</td>
<td>Advanced Digital Communication</td>
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**MODULES**

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<th>MODULE</th>
<th>Description</th>
<th>Contact Hours</th>
<th>Sem. Exam Marks (%)</th>
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<tbody>
<tr>
<td>1</td>
<td>Elements of digital communication systems, performance, communication channels and their characteristics, mathematical models for communications channels, Representation of band pass and low pass signals</td>
<td>8</td>
<td>15</td>
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<tr>
<td>2</td>
<td>Signal space representation of waveforms, vector space concepts, signal space concepts, Gram-Schmidt procedure, Bounds on tail probability, limit theorems for sum of random variables, complex random variables, random process</td>
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<tr>
<td>3</td>
<td>Representation of digitally modulated signals, memoryless modulation methods: PAM, PSK, QAM, Multidimensional signaling; orthogonal signaling, FSK, biorthogonal signaling, Signaling schemes with memory: CPFSK, CPM, Power spectrum of digitally modulated signals: PSD of digitally modulated signal with memory, PSD of CPFSK and CPM</td>
<td>7</td>
<td>15</td>
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<tr>
<td>4</td>
<td>Waveform and vector channel models: optimal detection for a general vector channel, MAP and ML receiver, decision regions, error probability, sufficient statistics. Waveform and vector AWGN channels, optimal detection for the vector AWGN channel, Implementation of optimum receiver for AWGN channels: The correlation receiver, the matched filter receiver.</td>
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<td>15</td>
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<tr>
<td>5</td>
<td>Characterization of band limited channels, Signal design for band limited channels. Design of band limited signals for no ISI-The Nyquist criterion, Design of band limited signal with controlled ISI-Partial response signaling</td>
<td>7</td>
<td>20</td>
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<tr>
<td>6</td>
<td>Optimum receiver with ISI &amp; AWGN: optimum maximum likelihood receiver, A discrete time model for a channel with ISI. Maximum-Likelihood Sequence Estimation (MLSE) for a discrete time white noise filter model detectors, turbo equalization, adaptive equalization, equalizer, decision feedback equalizer, recursive least squares algorithms, blind equalization</td>
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**END SEMESTER EXAM**
COURSE CODE | COURSE NAME | L-T-P:C | YEAR
---|---|---|---
04 EC 7113 | RECENT TRENDS IN COMMUNICATION ENGINEERING | 3 -0- 0: 3 | 2015

Pre-requisites: Nil

Objectives:

- To familiarize with modern trends in communication like software defined radio, cognitive radio, co-operative communication and IOT

Syllabus


Course Outcome:

Students finishing this course will have the ability

- to understand and analyse concepts of software defined radio and cognitive radio
- to make designs based on Cooperative communication concepts
- to analyse internet of things

References:

SOFTWARE DEFINED RADIO:

COGNITIVE RADIO:

COOPERATIVE COMMUNICATIONS:

THE INTERNET OF THINGS:
2. Adrian McEwen, Hakim Cassimally, Designing the Internet of Things, Wiley; 1 edition
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<th>COURSE CODE:</th>
<th>COURSE TITLE</th>
<th>CREDITS</th>
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<tbody>
<tr>
<td>04 EC 7113</td>
<td>Recent Trends in Communication Engineering</td>
<td>3-0-0:3</td>
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</table>

**MODULES**

| MODULE 1: Software radio concepts, Design principles, Receiver front end topologies, Noise and Distortion in RF chain, Object oriented software radios | 8 | 15 |
| MODULE 2: Direct digital synthesizers, CORDIC algorithm, Pulse shaping and interpolation filters, DDS with tunable DSM, Transmitter and receiver architectures | 6 | 15 |

**INTERNAL TEST 1 (MODULE 1 & 2)**


**INTERNAL TEST 2 (MODULE 3 & 4)**

| MODULE 5: Cooperative communications, Cooperation protocols, Cooperative communications with single relay-System model, Distributed space–time coding (DSTC), Distributed space–frequency coding (DSFC), Differential modulation for cooperative communications-Differential modulation, Energy efficiency in cooperative sensor networks- System model, Cognitive multiple access via cooperation- System model, Cooperative cognitive multiple access (CCMA) protocols | 7 | 20 |

**END SEMESTER EXAM**
Students have to register for the seminar and select a topic in consultation with any faculty member offering courses for the programme. He / She shall choose the topic based on the references from international journals of repute, preferably IEEE journals. A detailed write-up on the topic of the seminar is to be prepared in the prescribed format given by the Department. The seminar shall be of 30 minutes duration and a committee with the Head of the department as the chairman and two faculty members from the department as members shall evaluate the seminar based on the coverage of the topic, presentation and ability to answer the questions put forward by the committee.

Project work is to be carried out in the third and fourth semesters. Project work is to be evaluated both in the third and the fourth semesters. Based on these evaluations the grade is finalised in the fourth semester.

In Master’s Project Phase-I, the students are expected to select an emerging research area in the field of specialization. After conducting a detailed literature survey, they should compare and analyze research work done and review recent developments in the area and prepare an initial design of the work to be carried out as Master’s Project. It is mandatory that the students should refer National and International Journals and conference proceedings while selecting a topic for their Project. He/She should select a recent topic from a reputed International Journal, preferably IEEE/ACM. Emphasis should be given for introduction to the topic, literature survey, and scope of the proposed work along with some preliminary work carried out on the Project topic.

Project evaluation weights shall be as follows:-

Total marks for the Project: 150

In the 3rd Semester:- Marks:50
Project Progress evaluation:
Progress evaluation by the Project Supervisor : 20 Marks
Presentation and evaluation by the committee : 30 Marks
Students should submit a copy of Phase-I Project report covering the content discussed above and highlighting the features of work to be carried out in Phase-II of the Project. The candidate should present the current status of the Project work and the assessment will be made on the basis of the work and the presentation, by a panel of internal examiners in which one will be the internal guide. The examiners should give their suggestions in writing to the students so that it should be incorporated in the Phase–II of the Project.

**SEMMESTER IV**

<table>
<thead>
<tr>
<th>COURSE CODE</th>
<th>COURSE NAME</th>
<th>L-T-P:C</th>
<th>YEAR</th>
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<tbody>
<tr>
<td>04 EC 7294</td>
<td>PROJECT PHASE II</td>
<td>0-0-21:12</td>
<td>2015</td>
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</table>

In the fourth semester, the student has to continue the project work and after successfully finishing the work, he/she has to submit a detailed bounded Project report. The work carried out should lead to a publication in a National / International Conference or Journal. The papers received acceptance before the M.Tech evaluation will carry specific weightage.

TOTAL MARKS :100
Project evaluation by the supervisor/s : 30 Marks
Evaluation by the External expert : 30 Marks
Presentation & evaluation by the Committee : 40 Marks